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| 10/796,480 | 03/08/2004 | Daniel Lee Avery | US03 0080 | 2306 |

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

| EXAMINER | |
|---|---|
| TU, CHRISTINE TRINH LE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2138 | |

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/796,480 | AVERY ET AL. | |
| | Examiner | Art Unit | |
| | Christine T. Tu | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

***Double Patenting***

2. Claims 1, 2, 4, and 8 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12 and 13 of the copending Application No.10/796,484. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '484 substantially teaches the claimed invention. The copending application '484 does not explicitly teach the test signal sense circuit. The copending application '484, however, teaches the microcontroller is programmed to detect a test signal at one of the JTAG test nodes on JTAG signal paths (claim 13; at lines 2-3 of claim 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize the microcontroller of the copending application '484 would be comprises a test signal sense circuit. One having ordinary skill in the art would be motivated to realize so because the copending application '484 teaches that the microcontroller could detect a test signal of the test nodes on the signal paths (claim 13; at lines 1-3 of claim 12).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. Claims 14, 15, 16 and 17 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (12 & 13), 14, 15, and 17 of the copending Application No.10/796,484, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '484 substantially teaches the claimed invention. The copending application '484 does not explicitly teach the test signal sense circuit. The copending application '484, however, teaches the microcontroller is programmed to detect a test signal at one of the JTAG test nodes on JTAG signal paths (claim 13; at lines 2-3 of claim 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize the microcontroller of the copending application '484 would be comprises a test signal sense circuit. One having ordinary skill in the art would be motivated to realize so because the copending application '484 teaches that the microcontroller could detect a test signal of the test nodes on the signal paths (claim 13; at lines 1-3 of claim 12).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claims 23 and 26-27 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (19 & 23) and 21-22 of the copending Application No.10/796,484, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '484 substantially teaches the claimed invention. The copending

application '484 does not explicitly teach the feature of monitoring the JTAG I/O test nodes to detect connectivity to another inter-connectable circuit. However, the copending application '484 teaches that a microcontroller configures the JTAG test signals routing switches to route JTAG test signals between the first and second inter-connectable circuit arrangements via the JTAG output and input test nodes (claim 23, lines 6-8). It would have been obvious to one skilled in the art at the time the invention was made to realize that the microcontroller of the copending application '484 would encompassed the feature of monitor the JTAG I/O test nodes to detect the connectivity to another inter-connectable circuit. One having ordinary skill in the art would be motivated to realize so because the microcontroller (of the copending application '484) routes the JTAG test signals between the first and the second inter-connectable circuit arrangement via the JTAG I/O test nodes (as being recited at lines 7-8 of claim 23).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. Claim 29 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (12 & 13) of copending Application No. 10/796,484, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '484 teaches the claimed invention. The copending application '484 does not explicitly teach the test signal sense means. The copending application '484, however, teaches the

microcontroller is programmed to detect a test signal at one of the JTAG test nodes on JTAG signal paths (claim 13; at lines 2-3 of claim 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize the microcontroller of the copending application '484 would be comprises a test signal sense means. One having ordinary skill in the art would be motivated to realize so because the copending application '484 teaches that the microcontroller could detect a test signal of the test nodes on the signal paths (claim 13; at lines 1-3 of claim 12).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 112***

6. Claims 1-29 are again rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-7, 9, 11-14, 17-18, 21-23, 26 and 29:

The use of the phrase(s) "adapted to", "adaptively" and "adapted for" (throughout the claims) should be avoided because such a phrase does not provide positive limitation but only has the ability to perform so. In other words, it is not clear whether or not any functional limitation is actually being recited after each of the phrases "adapted to", "adaptively" and "adapted for".

Claim 9:

At lines 2-4, the phrase "a plurality of ... signal path switches adapted to route JTAG signals on the routing circuitry and between the routing circuitry and an external circuit" cannot be understood. Where exactly should the JTAG signals be routed? Where is the external circuit coming from? And how is the external circuit playing part of the circuit configurator arrangement.

Claims 8, 10, 15-16, 19-20, 24-25 and 27-28:

These claims are rejected because they depend on claims 1, 14 and 23 and contain the same problems of indefiniteness.

***Claim Rejections - 35 USC § 103***

7. Claims 1-10, 13-14, 16-18, 22-26 and 29 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Garreau (6,425,101).

Claims 1, 4, 6, 8 and 29:

Garreau discloses the invention substantially as claimed. Garreau discloses (figures 2 & 4) a test network (200) including a master controller (202) connected to a programmable switch (204 or 400). The programmable switch (204) is connected to a slave target device (206) containing JTAG compliant integrated circuits (IC1 through IC4). The master controller (20) further comprises a JTAG controller (210) and a switch controller (218) for providing JTAG test protocols by using an I/O line (211-1) and data to the slave target device (206), and receiving the test results by using the feed backward line (211-2) via the programmable switch (204 or 408) (figures 2 & 4, column 4 lines 41-column 5 line 36).

Garreau does not explicitly teach the controllable switches. Garreau, however, teaches (figure 4) that the programmable switch (400) comprises a plurality of vertical data lines (402) and programmably connected to horizontal data lines (404) forming a "crossbar" switch. Each of the horizontal data lines (404) is connected to one of the programmable switch I/O lines (410). Each of the programmable switch I/O switch I/O lines (410) are in turn connected in a pair-wise manner to the ICs (IC1 through IC4) located on the target hardware device (206) such teach each IC can be selectively tested (column 6 lines 49-column 7 lines 28).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's combination of plurality of vertical data lines (402) and the plurality of the horizontal data lines (404) (in Garreau's programmable switch [208]) would have been the controllable switches. One having ordinary skill the in the art would be motivated to realize so because Garreau's combination of vertical data lines (420) and horizontal data lines (404) are used for selectively connecting a IC [in the target device (206)] to the master controller (202) (column 7 lines 12-28).

Claim 2:

Garreau also teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable switch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Claim 3:

Garreau does not explicitly teach a memory for storing the corresponding configuration data before sending such configuration data to the master controller (704). However, it would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's host computer (702) would have comprised a memory for storing such configuration data. One having ordinary skill in the art would be motivated to realize so because having a memory for storing (configuration) data inside a computer (or a host computer) is well-known in the art.

Claim 5:

Garreau does not explicitly teach a memory for storing control signals. Garreau, however, teaches that the JTAG controller (210) provides/sends JTAG test protocols used by JTAG test circuitry (figure 2, column 4 lines 60-65).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's JTAG controller (210) would have comprised a memory for storing JTAG test protocols for sending them out to the test circuitry. One having ordinary skill in the art would be motivated to realize so because using a memory to store certain data before sending such data out would have been a matter of design choice and such a choice would not affect the result of the testing on a circuit.

Claim 7:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2) (figure 4, column 8 lines 48-58; column 5 lines 10-36).

Claim 9:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2). In this way the integrated circuits (IC3 and IC2) can be tested and are daisy-chained in the JTAG path in responsive to the appropriate switch control signal from the switch controller (218) (figure 4, column 8 lines 32-58; column 5 lines 10-36).

Claim 10:

Garreau also teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable switch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Claim 13:

Garreau further teaches that the JTAG controller (210) provides/sends JTAG test protocols including test vectors used by JTAG test circuitry via the I/O line (211-1) (figure 2, column 4 lines 60-65).

Claims 14 & 18:

Claims 14 and 18 are rejected for reasons similar to those set forth against claims (1 & 5) and (2 & 5).

Claim 16

Garreau further teaches (figure 4) that the programmable switch (400), which is controlled by the JTAG controller (210) and the switch controller (218), comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2). In this way the integrated circuits (IC3 and IC2) can be tested and are daisy-chained in the JTAG path in responsive to the appropriate switch control signal from the switch controller (218) (figure 4, column 8 lines 32-58; column 5 lines 10-36).

Claim 17:

Garreau's master controller (704) directs the programmable switch (706) to selectively couple an IC in responsive to the configuration data from the host computer (702) (figure 7, column 8 lines 62-62).

Claim 22:

Garreau does not explicitly teach an analog-to-digital converter (ADC) (in the configurator arrangement) for converting analog signal to digital signal. It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's test network (200) would have been comprised of an A/D converter. One having ordinary skill in the art would be motivated to realize so because the use of an A/D converter for converting analog data into digital data is well-known in the art.

Claims 23 and 26:

These claims are similar to claims 1-3 except that the feature of mentoring the JTAG I/O test nodes to detect connectivity to another inter-connectable circuit is being recited.

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's JTAG controller (210) would encompassed the feature of monitor the JTAG I/O test nodes to detect the connectivity of the ICs. One having ordinary skill in the art would be motivated to realize so because Garreau's JTAG controller (210) is capable of testing only the integrated circuit IC1 after the switch

controller (218) directs the programmable switch (204) to connect an I/O line (211-1) to a feed forward line (220) and the feed backward line (222) to an I/O line (211-2) (figure 2, column 5 lines 26-36).

Claims 24-25:

Garreau's configuration data is provided to the master controller (704) which directs the programmable switch (706) to selectively couple the IC (708) to the master controller (704) (figure 7, column 8 line 57-column 9 line 5).

***Response to Arguments***

8. Applicant's arguments filed July 11, 2006 have been fully considered but they are not persuasive.

The applicant states that he will respond to the provisional obviousness-type double patenting rejection if the copending application is issued as a patent prior to the present application. In other words, the applicant has not been resolved the rejection of provisional obviousness-type double patenting. Therefore, the provisional obviousness-type double patenting rejection still stands for reasons set forth above (¶ 2-5).

The applicant also argues that Garreau reference does not teach or suggest the limitation of a test-signal sense circuit/means nor control logic circuit (for claims 1, 14, 29 and 23). Examiner, however, disagrees against applicant's remark. Such limitation is shown by Garreau. Garreau's I/O lines (211-1 and 211-2) provide test protocols and

test vectors under the JTAG controller (210), used by corresponding test circuits to assess whether the integrated circuit being tested is functioning properly (figure 2, column 4 lines 56-66).

Also for claim 23, applicant further argues that Garreau does not teach the routing of JTAG test signals on an inter-connectable circuit board. Garreau does teach such limitations. Garreau teaches that the programmable switch (204) routes test signals between an IC1 and the JTAG controller (210).

For claims 6 and 16, applicant alleges that Garreau reference does not teach the limitations of detecting test signals passing between the configurable test signal routing paths and an external circuit. Garreau does teach such limitations. Garreau teaches test vectors and being routed via the programmable switch (204) to a master controller (and such a master controller is located outside of Garreau's slave target device (206) (figure 2, column 4 lines 56-66).

For claims 23 and 24, applicant further alleges that Garreau reference does not teach the limitations being directed to JTAG signal path switches adapted to route JTAG signals between a configured circuit and other configured circuits as claimed. However, such limitations are taught by Garreau. Garreau does teach two inter-connectable circuit boards [Garreau's master controller (202) and slave target device (206)]. Such

Garreau's master controller (202) and the salve target device (206) do communicate to each other by using the programmable switch (204) (figure 2).

For claim 18, the Garreau reference does not teach the limitations directed to computer-executable code being received from the user interface via the communication port and then stored in memory. Garreau does not teach the JTAG controller (210) provides/sends JTAG test protocols including instructions, used by JTAG test circuitry (figure 2, column 4 lines 60-66).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's network (200) would have been comprised of an user interface and Garreau's JTAG controller (210) would have been comprised a memory. Such a user interface would provide JTAG test protocols to such a memory [in Garreau's JTAG controller (210)] so that the JTAG protocols can be sent from Garreau's JTAG controller (210) to the test circuitry. One having ordinary skill in the art would be motivated to realize so because using a user interface for providing test protocols and a memory to storing such test protocols before sending such data out would have been a matter of design choice and such a choice would not affect the result of the tes6ting on a circuit.

For claim 22, Garreau does not explicitly teach an analog-to-digital converter (ADC) (in the configurator arrangement) for converting analog signal to digital signal. It would have been obvious to one skilled in the art at the time the invention was made to

realize that Garreau's test network (200) would have been comprised of an A/D converter. One having ordinary skill in the art would be motivated to realize so because the use of an A/D converter for converting analog data into digital data is well-known in the art.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christine T. Tu
Primary Examiner
Art Unit 2138

October 3, 2006